ISSN:2229-6107

INTERNATIONAL JOURNAL OF PURE AND APPLIED SCIENCE & TECHNOLOGY

E-mail :
editor.ijpast@gmail.com
editor@ijpast.in

www.ijpast.in

INTERNATIONAL JOURNAL OF PURE AND APPLIED SCIENCE & TECHNOLOGY
IJPAST

ISSN 2229-6107
www.ijpast.in
Vol 13 ,Issue 4.Oct 2023

SINGLE-PHASE SPLIT-INDUCTOR DIFFERENTIAL BOOST INVERTERS

ANUSHA AVULA$_1$, Y. RAJASEKHAR REDDY$_2$

ABSTRACT:

Multilevel inverter configurations are a suitable candidate for medium and high power applications. This study presents a new one-capacitor-based five-level (2Vdc, Vdc, 0, −Vdc, − 2Vdc) boost multilevel inverter. The single-phase version of the proposed formation has one dc-source, eight switches and one capacitor. To provide boosting ability, the inverter is operating based on charge-pump theory, where the capacitor is charging in parallel and discharging in series connections to provide a higher output voltage. The proposed configuration requires simple control tasks, and for this purpose, level-shift pulse width modulation strategy, where the reference signal is compared with four carriers, is implemented to drive the switches and generates the required pulses pattern. The developed inverter has some distinct features like the usage of only one dc-source and one-capacitor, compact size, simple control requirements and boosting ability. The system is simulated with MATLAB/ Simulink and a hardware prototype is developed to verify the performance of the developed five-level configuration. The results show that the developed five-level multilevel inverter reaches the expected performance

INTRODUCTION

Multilevel inverters (MLIs) have emerged and evolved as a perfect solution for the medium and high voltage/power applications where high-quality dc-ac power conversion is needed. The classical topologies for the MLIs are neutral point clamped (NPC), flying capacitor (FC) and cascade H-bridge (CHB). These topologies are widely researched and are well established in industrial applications. However, for a higher number of output levels, the increased in the number components required for NPC and FC becomes quixotic. Similarly, for CHB, the higher number of isolated dc voltage sources for a higher number of levels limits its applications [1]–[5]. One category of the MLI topologies has been based on the multiple isolated dc voltage sources. In this category

PG SCHOLAR$_1$, ASSOSCIATE PROFESSOR AND HOD$_2$

DEPARTMENT OF EEE, MOTHER TERESA INSTITUTE OF SCIENCE AND TECHNOLOGY, SANKETIKA NAGAR, KOTHURU, SATHUPALLY, TELANGANA 507303

ISSN 2229-6107
www.ijpast.in
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the topologies have been classified as symmetrical and asymmetrical configured topologies. In symmetrically configured topologies, the dc voltage sources have the same magnitude. In asymmetrically configured topologies, the dc voltage sources have different magnitude resulting in a higher number of levels with a lower number of switches as well as dc voltage sources. In both types of topologies, the need for a higher number of isolated dc voltage sources limits their applications [6]–[9]. In order to reduce the number of dc voltage sources, the use of topologies with switched capacitor (SC) units have been recommended. The SC unit has been used with different arrangements resulting in different output voltage levels. One topology based on capacitors has been proposed in [10] and named as packed E-cell (PEC) topology. With two dc voltage sources and two capacitors, a nine-level output voltage waveform can be achieved, however, the topology lacks the boosting of the input voltage. Similar to [10], nine-level MLI topologies with two dc voltage sources and two capacitors have been proposed in [11], [12]. The authors in [13] proposed two new topologies with two dc voltage source along with two capacitors. Both topologies generate nine levels of the voltage across the load. However, both topologies use H-bridge for the polarity change, which requires switches with a higher voltage rating. The topologies also lack boosting ability. A K-type topology has been proposed in [14] in which two dc voltage sources along with two capacitors have been used for 13 levels at the output. However, the rating of both capacitors is different. In addition, both capacitors need to discharge for the last three levels, which results in a nonsteady response in the capacitor voltage and unequal voltage steps across the load. Most of the SC-based topologies use single dc voltage source and the SC units are used to create different dc-link voltages for the multilevel output across the load. Some of the topologies with SC units have a distinctive feature of boosting the output voltage, i.e., the peak of the output voltage is higher than the input supply. The SC-based MLI topology based on H-bridge has been proposed in [15], and [16] in which SC is connected through H-bridges for charging and discharging purposes. Several H-bridge with SC can be connected for a higher number of levels, which increases the number of switches. A new seven-level boost inverter topology has been proposed in [17] with triple voltage gain. A hybrid

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switchedcapacitor based nine-level MLI topology has been proposed in [18], however, the boosting feature is absent from the topology of [18]. Few more seven-level boost inverter topologies have been proposed in [19]–[25], however, the higher number of components have always been the major concern about these topologies. Furthermore, the topologies proposed in [21], [22], [24], [25] have a lower value of boosting factor. Based on the twice boosting gain, several nine-level MLI topologies have input. In [26], a single-stage nine-level topology has been proposed. The topology uses 12 switches for nine levels across the load with twice of voltage gain. An improvement in terms of switches from [26] has been made in [27], which uses 11 switches to achieve nine levels. In [28], a new nine-level boost topology based on SC has been proposed to which the capacitors are charged in the first two levels and then discharged to give the boost feature in the next two states of the output voltage. Furthermore, for the topologies [29]–[38] the switch count for nine levels has been on the higher side. Considering these facts, this paper attempts to synthesize a nine-level voltage using the SC technique to reduce the component count. The main features of the proposed MLI are:

- A single dc source is used.
- Self-voltage balancing is achieved across the capacitors.
- The output voltage is twice the input voltage.
- Low voltage stress across the switches.
- The capacitor voltages are independent of the load power factor and modulation index.

PROPOSED TOPOLOGY

A. CONFIGURATION OF THE PROPOSED TOPOLOGY The configuration of the proposed single-phase SCMLI topology is shown in Fig. 1 along with the maximum voltage stress across each switch as a factor of input dc voltage source, i.e. Vdc. The assembly of the proposed topology consists of ten switches. The switches can be either IGBT or MOSFET based on the frequency of operation, voltage, and power rating of the converter. Two capacitors C1 and C2 are used to split the dc supply voltage into halves. By systematic and sequential turning ON/OFF of the switches, the capacitor voltages are maintained at half of the supply voltage, i.e., Vdc/2. The proposed topology generates nine levels across the load with a twice voltage boosting factor. The switching

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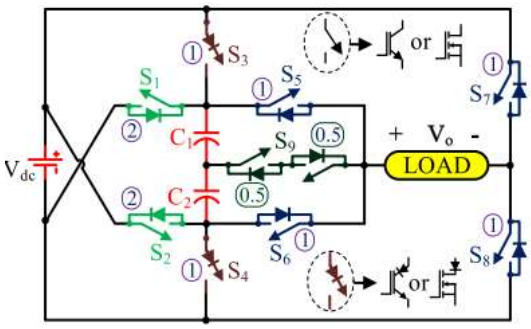

Fig. 1 General Schematic representation of proposed NINE - level inverter

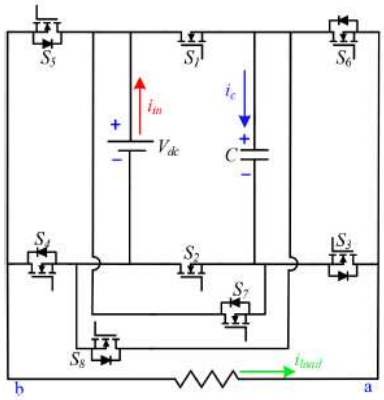

Fig. 2 Single-phase configuration of the proposed five-level inverter

Three-phase power output. The output voltage of the suggested design is more than double the input voltage, which is an advantage over the arrangement presented in [25, 26]. Using only a single dc-source, a single capacitor, and eight power switches, the suggested arrangement may provide a five-level output voltage with an amplitude twice that of the input voltage. The range of generated voltages is from -2Vdc to +2Vdc. Figure 1 is a high-level schematic depiction of the proposed system. Adding three capacitors and 24 power switches allows the system to be scaled up to a three-phase configuration. Only the single-phase setup will be analyzed and explored here. In certain configurations, the capacitor is linked in parallel with the dc-source during charging. To get a 2Vdc output voltage level, it is disconnected from the dc-source and rejoined in series with the source. In this research, level-shift pulse width modulation (LS-PWM) is used to control the switches of a multilevel inverter. The necessary switching states are produced by comparing the reference voltage to four carriers.

This research is structured as follows: The several modes of operation of the multilayer boost-inverter are discussed in Section 2. In Section 3, we'll go through our modulation technique; in Section 4, we'll calculate the losses brought on by our suggested setup; and in Section 5, we'll provide our findings from both simulation and experimentation.

Multilevel inverter with two proposed boost levels

In Fig. 2, we can see the five-level boost multilevel inverter that was presented. The output voltage is double the input voltage in the suggested design, which is a five-level multilevel inverter with boosting capability. Only eight switches are used in the designed topology, with two of those switches lacking an anti-parallel diode. However, only six valid switching states are implemented in order to provide the five-level output voltage, as shown in Table 1. Figures 3 and 4 show all the possible operating states.

2.1 Modes of Operation

In the first, "freewheeling," mode, the inverter outputs 0 V and the dc-source charges capacitor C (Fig. 3a). This study assumes the capacitor is charged when a big inrush current is pulled from a dead

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capacitor at zero voltage. In fact, this is a problem for any multi-tiered architecture that makes use of FCs. A precharge device, which permits the capacitor voltage to rise up gradually, might be used in high power applications [27-32]. The switches labeled S1, S2, S3, and S4 are all turned on. The voltage across capacitors C is the same as the voltage across the dc source since C is being charged by the dc source. The input voltage charges capacitor C, and the steady-state value of capacitor C is equal to the input voltage. The a and b output terminals are linked together.

In Mode 2, with just S1, S2, S3, and S5 activated, the inverter produces an output voltage equal to the input voltage (Fig. 3b). The voltage across capacitors C is the same as the voltage across the dc source since both are charged from the same source. The positive terminal of the input source is linked to terminal b of the output, while the negative terminal of the dcsource is connected to terminal a.

In Mode 3, switches S3, S5, and S8 are on, while the rest of the switches are off, causing the inverter to produce an output voltage that is double the input voltage (see Fig. 3c). Terminal b of the output is wired to the + terminal of the dc-source, while terminal an is wired to the - terminal of capacitor C.

In freewheeling mode 4 (see Fig. 4a), the inverter's output voltage is zero, and the dc-source charges capacitor C. The switches labeled S1, S2, S3, and S4 are all turned on. The voltage of C is identical to the voltage of the dc source since it is charged directly from the dc source. The input voltage is used to charge capacitor C, and the steady-state value of C is the same as the input voltage. The second output terminal (b) is wired to the first (a).

In mode 5, all except switches S1, S2, S4, and S6 are on, and the inverter produces an output voltage equal to the input voltage (see Fig. 4b). Voltage in C is constant since it is being charged by the dc source. Terminal b of the output is wired to the negative end of the dc source, whereas terminal an is wired to the positive end.

In mode 6, switches S4, S6, and S7 are on, while the other switches are off. This mode causes the inverter to produce an output voltage that is double the input voltage (see Fig. 4c). The positive terminal of capacitor C is linked to terminal a, while the negative terminal of the dc-source is connected to terminal b, the output.

2.2 Parameterized layout

Capacitance selection is critical to minimizing ripple voltage, since excessive ripple might result in uneven voltage steps at the output. C is charged in parallel with the dc source, as shown in Figures 3a, b, and 4a. The resulting characteristic equations are as follows:

$$\{v_c = v_{dc} \Leftrightarrow i_c = i_{in} \quad (1)$$

The charging process for C is ongoing in the configuration shown in Fig. 4a. Its present equation, however, differs from its historical one and may be labeled as

$$\{v_c = v_{dc} \Leftrightarrow i_c = i_{in} - i_{load} \quad (2)$$

The characteristics equation of the capacitor when C is discharging in the modes shown in Figures 3c and 4b is

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ISSN 2229-6107
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$$\{v_c = v_o - v_{dc} \Leftrightarrow i_c = i_{in} \quad (3)$$

Fig. 5 shows a graph showing the voltage across a capacitor. C might be chosen in the following ways based on the graph and equations (1-3):

Table 1 Switching states of the five-level inverter

Vector	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	Output
V_0	1	1	1	1	0	0	0	0	0
V_1	1	1	1	0	1	0	0	0	V_{dc}
V_2	0	0	1	0	1	0	0	1	$2V_{dc}$
V_3	1	1	1	1	0	0	0	0	0
V_4	1	1	0	1	0	1	0	0	$-V_{dc}$
V_5	0	0	0	1	0	1	1	0	$-2V_{dc}$

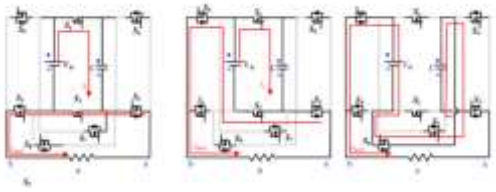

Fig. 3 Operation modes
Mode I, (b) Mode II, (c) Mode III

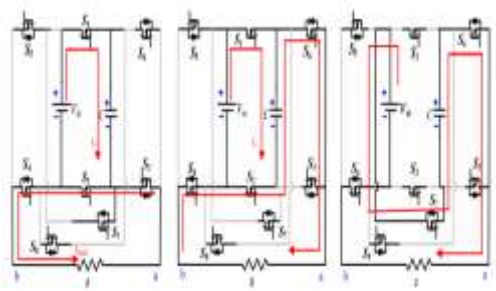

Fig. 4 Operation modes
(a) Mode IV, (b) Mode V, (c) Mode VI

$$C = \left(\frac{v_o - v_{dc}}{2\Delta v_c}\right) DT_s \quad (4)$$

Input voltage vdc, output voltage vo, sampling time Ts, allowable ripple in capacitor voltage vc, and duty ratio D are all inputs into the equation that yields C.

Table 2 provides a summary of the component voltage and current stresses. The current pressures on each switch are about the same.

However, there seems to be a variety of voltage stressors. The largest voltage stress is seen in S7 and S8, which is coincident with the output voltage. On the other switches, the voltage stress is proportional to the input voltage. The voltage strains on switches S7 and S8 are greater than those on the other switches because of the asymmetry in the circuit.

Therefore, component selection requires careful consideration.

PWM with a third level of level shifting

PWM is often used to control the switching frequency of power converters (dc or ac converters). Pattern of Pulses

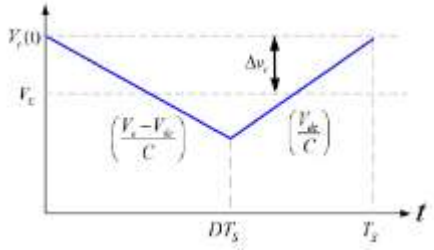

Fig. 5 Capacitor voltage illustration

The PWM block is designed to produce a waveform with a low harmonic content and a high modulation index. As an added bonus, modulation techniques may be tailored to lessen the effects of switching losses, current ripple, and capacitor voltage imbalance. The switching in a two-level converter is generated by comparing a single triangular carrier to a modulation signal.

Table 2 Devices voltage and current stress

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Device	Voltage stress	Current stress
S_1	V_{in}	I_{in}
S_2	V_{in}	I_{in}
S_3	V_{in}	I_{in}
S_4	V_{in}	I_{in}
S_5	V_{in}	I_{in}
S_6	V_{in}	I_{in}
S_7	V_0	I_{in}
S_8	V_0	I_{in}

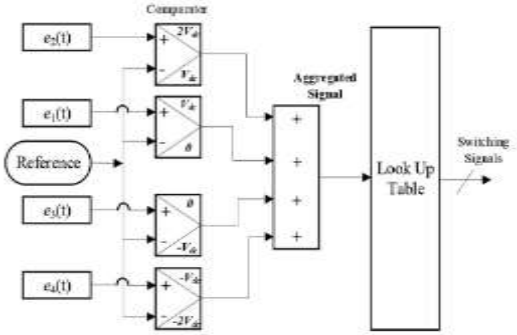

Fig. 6 Switching signal generation schematic diagram

phase-modulated signal is compared to multi-triangular carriers in multi-level topologies. Multicarrier modulation may be broken down into phase-shifted pulse-width modulation carriers and low-skew pulse-width modulation carriers.

The five-level inverter suggested here is controlled by LS-PWM produced specifically for this research. In Fig. 6, we see a schematic depicting the overarching design for how switching signals for the inverter switches are generated. N-level inverters, as stated in [33], need (N 1) different carrier waveforms in addition to a reference signal. As can be seen in Fig. 7, four carriers are used since the suggested topology has five levels. The comparison of the carrier signals to a sinusoidal reference waveform establishes the switching pattern. All four carriers have the identical amplitude, phase shift, and switching frequency for perfect symmetry.

There are four distinct industries that correspond to the modulation process. Sector 1 compares the reference signal to the carrier signal e3, which results in an output value between 0 and Vdc. The output voltage in sector 2 ranges from Vdc to 2Vdc, and is generated by comparing the reference signal with the carrier signal e4. The suggested seven-stage boost converter functions symmetrically. The same method is used to depict the up half of the cycle.

The multilayer inverter's switching patterns are shown in Fig. 8.

4-Problem-solving examination of a loss

When a switching device conducts, it experiences losses known as conduction losses; when it switches, it experiences losses known as switching losses.

Each of the eight potential switching states has at least three switches activated. These results in two distinct forms of energy waste: conduction losses and switching losses. Analytical computation of switching and conduction losses will be covered in the following sections.

4.1 Losses due to conduction

Two of the eight switches in the proposed topology are power switches that can conduct in only one way while the other six can only block in one direction.

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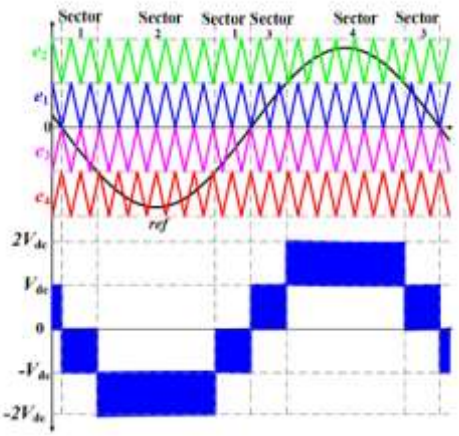

Fig. 7 LS-PWM scheme

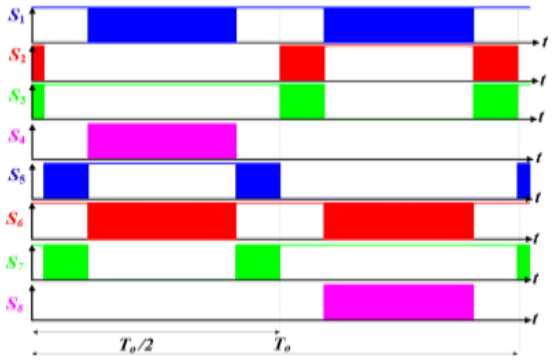

Fig. 8 Driving signals of the five-level inverter

Bidirectional conducting, the instantaneous conduction losses of the
Power switch and its body diode can be given as [14, 24]

$$\rho_{c,T}(t) = \left[V_T + R_T i_L^{q}(t)\right] i(t) \qquad (5)$$

$$\rho_{c,D}(t) = \left[V_D + R_D i(t)\right] i(t) \qquad (6)$$

The average conduction losses are expressed as

$$\rho_{c,avg} = \frac{1}{\Pi}\int_0^{\Pi} \left[\begin{matrix} \{N_T(t)V_T + N_D(t)V_D\} i_L(t) \\ + \{N_T(t)R_T i_L^{q+1}(t)\} + \{N_D(t) i_L^2(t)\} \end{matrix} \right] d(\omega t) \qquad (7)$$

where c,T(t), c,D(t), VT, VD, RT, RD,, ND, NT, and c, avg(t) represent the instantaneous conduction losses of the transistor, diode, equivalent on-resistance, number of conducting diodes, number of conducting transistors, constant given by transistor characteristics, and instantaneous and average conduction losses, respectively.

Switching losses, 4.2%

A linear approximation of the switching period voltage and current may be used to determine the switching losses of each switching device [14, 24]. Losses in starting energy may be determined via the formula

$$E_{on,j} = \int_0^{t_{on}} \left\{ \left[V_{o,j} \frac{t}{t_{on}} \right] \left[-\frac{I}{t_{on}}(t - t_{on}) \right] \right\} dt = \frac{1}{6} V_{o,j} I t_{on} \qquad (8)$$

Similarly, energy losses of the *j*th switch during turning off are
Calculated as

$$E_{off,j} = \int_0^{t_{off}} \left\{ \left[V_{o,j} * \frac{t}{t_{off}} \right] \left[-\frac{I}{t_{off}}(t - t_{off}) \right] \right\} dt = \frac{1}{6} V_{o,j} I t_{off} \qquad (9)$$

to which Eon,j, ton, I, Vo,j Eon,j, and ton represent the turn-on loss of the jth switch, the turn-on time, the switch current after turning on, the switch voltage while turning off, the turn-off loss of the jth switch, and the turn-off time.

The overall power lost while switching may be computed as

$$\rho_S = \sum_{j=1}^{2n+2} \left[\frac{1}{6} V_{o,j} * I(t_{on} + t_{off}) f_j \right] \qquad (10)$$

Fig. 9 shows a graph showing the inverter's efficiency. The suggested

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inverter functions well in a power range of 350 W to 650 W. However, its efficiency is more than 95% in all power ranges up to 800 W.

5 Discussions and Results

The system is simulated in MATLAB/Simulink and a hardware prototype is constructed in the lab to validate the operation in a variety of circumstances.

The Outcomes of the Simulations, Version 5.

Input voltage is kept constant at 200 V and switching frequency is maintained constant at 5 kHz throughout the simulation. The simulation framework has been used to investigate a wide variety of use cases. Figure 10 shows the connection between input current and capacitor current. It is important to remember that an inrush charging current is produced each time capacitor C is charged. Observe Fig. 10 to see this phenomena in action. As a result, the suggested topology is more suited to low-power uses.

With just one capacitor and one dcsource, the suggested topology has a clear benefit over other topologies in the literature since balancing control is unnecessary. There is no output filter between the inverter and the resistive load in Fig. 11.

Both the output voltage and current have five distinct settings (off, 0 volts, 2 volts, -2 volts, and -2 volts). As can be seen in Fig. 12, the total harmonic distortion (THD) in this instance is around 34%. Filtering it out might bring it down to a more reasonable level, even when compared to three- or even two-tiered setups.

Case study with an inductive load linked to the inverter terminals is shown in Fig. 13. The output current is smoothed because of the inductive load, but no output filter is needed, as in the resistive load case. As can be observed in Fig. 14, the THD of the output current is around 5.14%.

5.2 Observations from Experiments

Figure 15a depicts a high-level schematic depiction of the implemented hardware setup, and Figure 15b depicts a photocopy of the actual system. The LS-PWM is implemented in DSpace 1202 to provide the gating signals for the power switches. To create the five-level multilevel inverter, eight IRFP264 power MOSFETs are employed.

In Fig. 16, we have a case study in which the input voltage is increased to 60 V and a resistive load is attached to the inverter's terminal.

The output voltage is around 120 V. Figure 17 shows the fast Fourier transform of the measured output current with a resistive load, which may be used to get the output current's total harmonic distortion (THD).

THD is below 25% without a filter, as seen in Fig. 17

The experimental waveforms of the L-R loaded prototype are shown in Fig. 18. Nothing is filtered out. Inducing a load aids in

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ISSN 2229-6107
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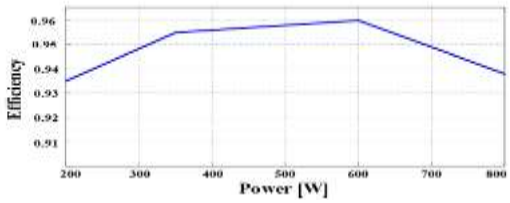

Fig. 9 Estimated efficiency of the proposed five-level multilevel inverter

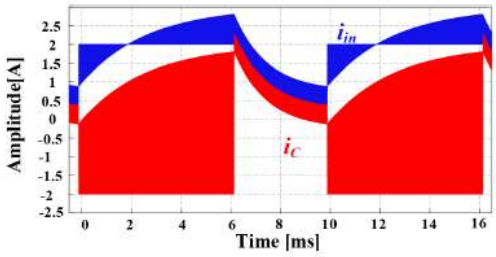

Fig. 10 Characteristics of input current and capacitor current

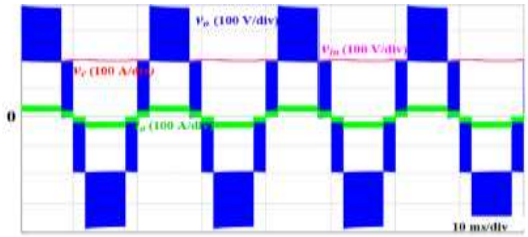

Fig. 11 Output voltage, output current, input voltage and capacitor voltage, with resistive load, R = 200 Ω

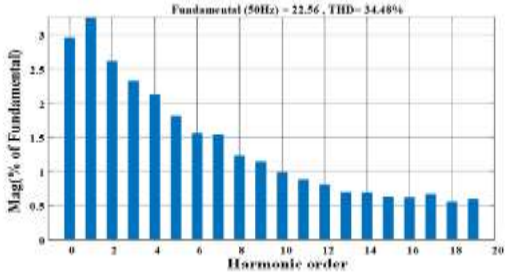

Fig. 12 THD of output current with resistive load and no filter is added

Tamp down the harmonics of the stream. THD of the output current is lowered to 8% as a result.

Table 3 shows a comparison between the suggested five-level boost inverter and other five-level topologies already available in the literature. NPC necessitates eight power switches and five capacitors but still lacks the capacity to raise voltage, leading to a lower output voltage than input. FC five-level inverters have the same number of components as NPC ones, but only need three capacitors rather of five. CHB inverters don't need capacitors, but they do need a lot of separate dc power sources. The table shows that the suggested arrangement may provide a five-level output with boosting capability, with an output voltage that is twice as high as the input voltage, and using the fewest possible parts.

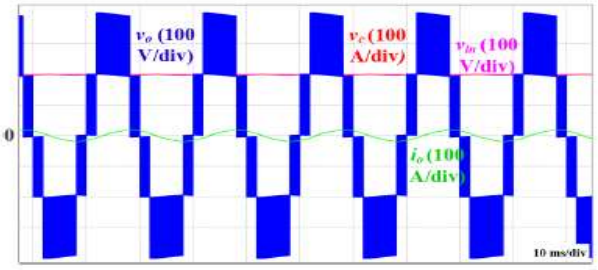

Fig. 13 Output voltage, output current, input voltage and capacitor voltage, with inductive load, R = 10 Ω and L = 5 mH

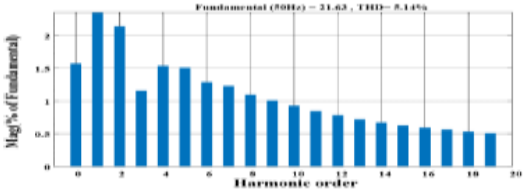

Fig. 14 THD of output current with inductive load and no filter is added

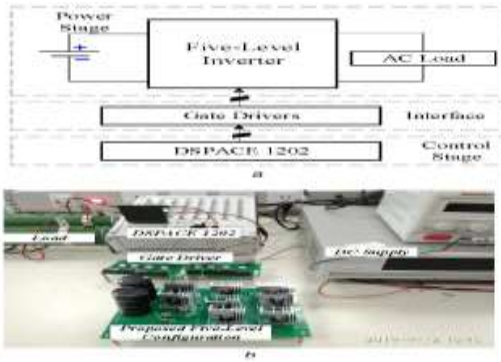

Fig. 15 Experimental setup
Block diagram, (b) Photograph of prototype

INTERNATIONAL JOURNAL OF PURE AND APPLIED SCIENCE & TECHNOLOGY
IJPAST
ISSN 2229-6107
www.ijpast.in
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Sixthly, Wrap-Up

In this paper, a boost multilevel inverter with five stages was described. The designed arrangement for a single-phase version is made up of eight switches and a single dc-capacitor. An output of up to five levels may be produced at an amplitude more than double the input voltage.

Since just one capacitor is used, there is no need to worry about the balance problem occurring.

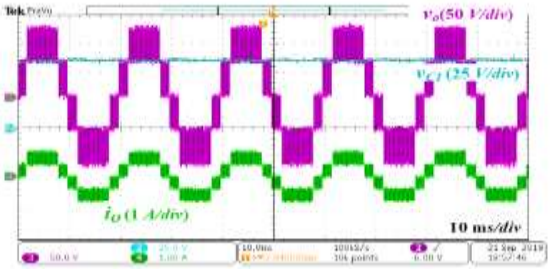

Fig. 16 Measured output voltage, output current and capacitor voltage with resistive load and no output filter, R = 50 Ω

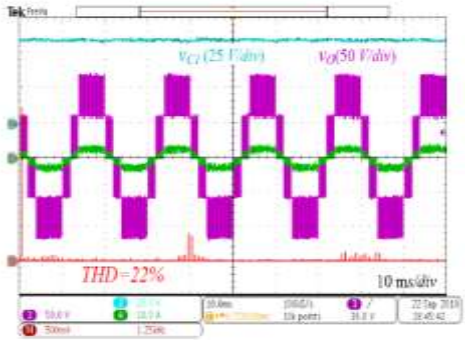

Fig. 17 Measured THD, output voltage, output current and capacitor
Voltage with resistive load and no output filter R = 50 Ω

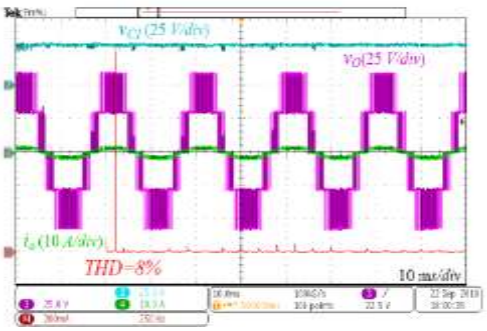

Fig. 18 Measured THD, output voltage, output current and capacitor
Voltage with inductive load and no output filter, R = 10 Ω and L = 3 mH

The suggested inverter has an advantage over existing alternatives due to its boosting function, which may be used in PV systems. After being charged by the dc-source, the dccapacitor is switched into series with the power supply. This means a greater output voltage is possible. LS-PWM is used to power the inverter's switch drivers.

The switching states are planned so that the capacitor has enough time to charge, preventing significant voltage fluctuations.

Table 3 Component requirements for single-phase five-level multilevel inverter

Topology	NPC [34]	FC [19]	CHB [35]	[10]	[36]	Diode clamped [37]	Capacitor clamped [38]	This work
number of main switches	8	8	8	4	5	8	12	8
number of diodes	0	0	0	4	4	6	0	2
number capacitors	3	3	0	2	2	4	4	1
number of dc-source	1	1	2	1	1	1	1	1

The proposed system is tested through simulation in the MATLAB/SIMULINK environment and hardware prototyping in the lab. The analytical findings are in agreement with the simulation and experimental results.

CONCLUSION

A new single-phase nine-level MLI topology has been proposed in this paper. The proposed nine-level boost inverter topology has been based on switched capacitors with a reduced number of switches. A detailed comparative study highlights the proposed topology potential in terms of reduced requirements of components for the same number of

ISSN 2229-6107
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voltage levels. The cost comparison supplements the lower price of the proposed topology with a single dc voltage source for nine-level and proves it to be cost-beneficial. The efficiency comparison also gives the additional edge of the proposed topology compare to other topologies. The reduction in the number of components, cost, and higher efficiency makes the proposed topology suitable for low and medium voltage applications. The workability of the proposed topology has been proved by the different results with various loading conditions. The different simulation and hardware results verify the improved performance of the proposed topology

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